AW-CU544

IEEE 802.11 b/g/n MAC/baseband/radio and Bluetooth 5.2 IoT Module

Reference Design Guide

Rev. A

(For Standard)

Revision History

Version	Revision Date	Description	Initials	Approved
A	2022/11/06	● Initial Version	Steven Jian	Chihhao Liao

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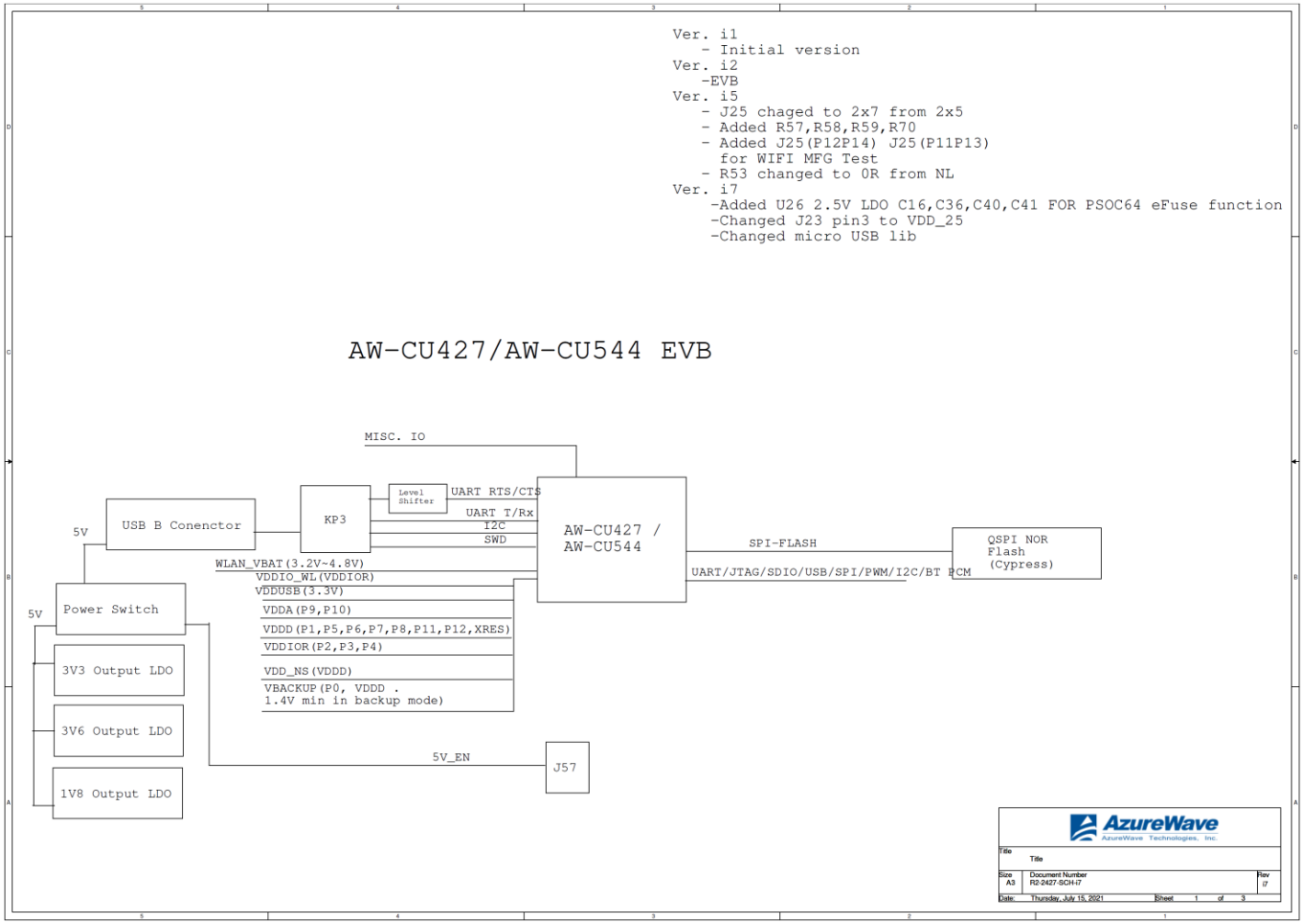
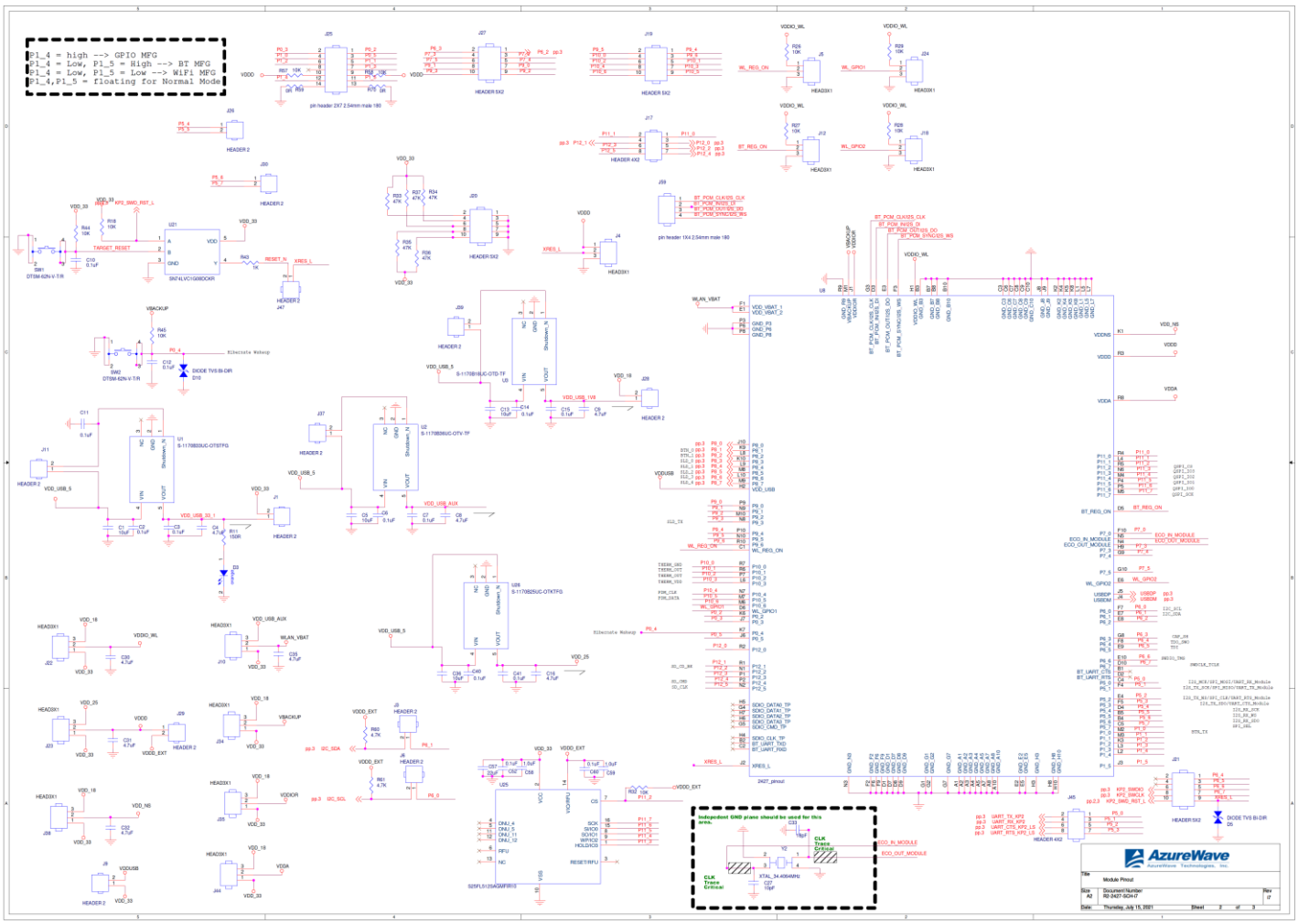
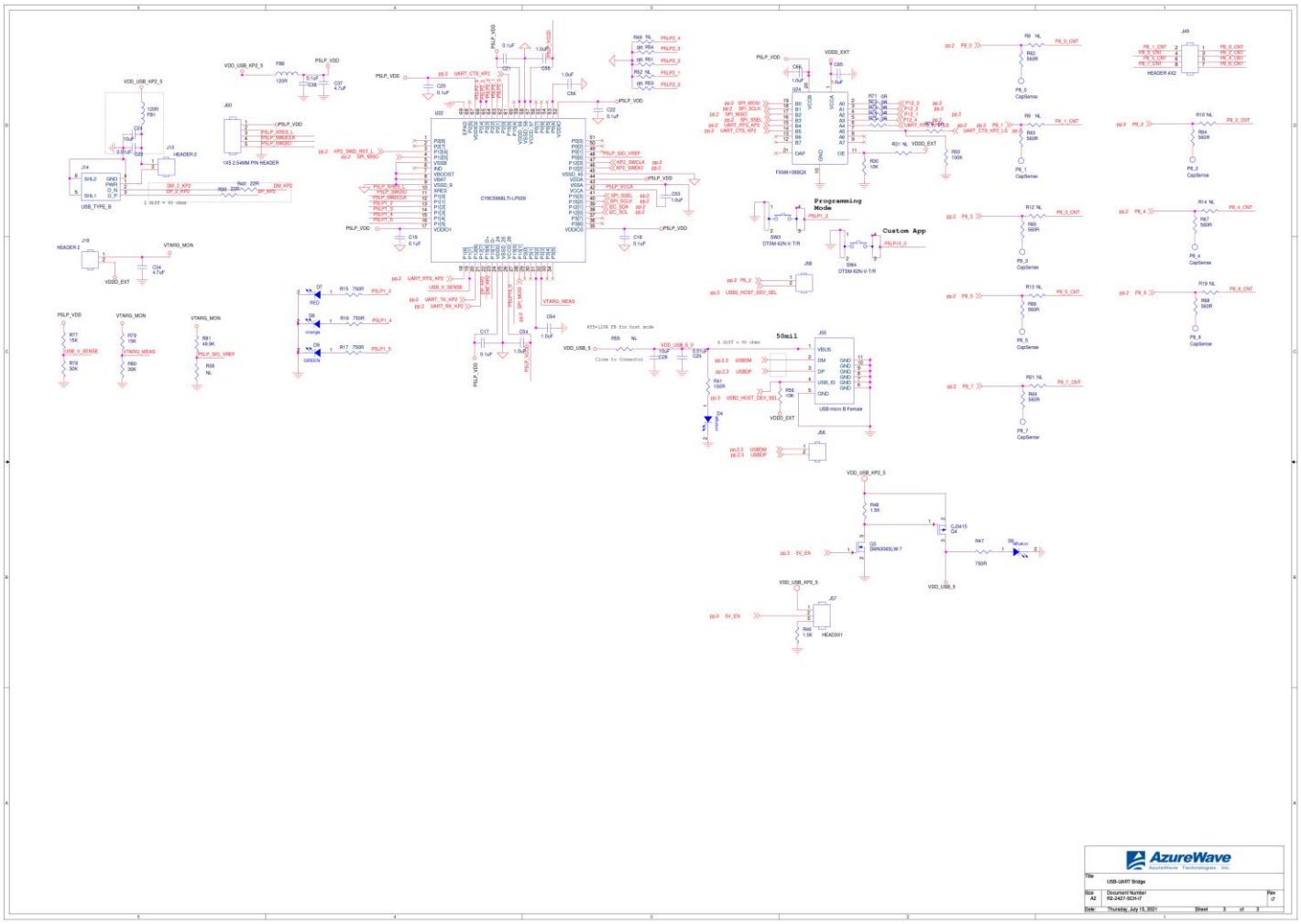
1. Reference Schematic

Values (ex. capacitance, inductance, etc.) in the reference schematic are for reference only







2. Design Considerations

2.1 Power Supply

Keep noise sensitive power rail VDDA from other power/signal nets

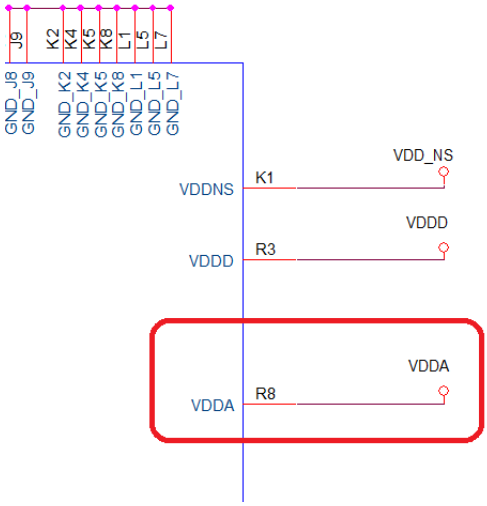


Figure 1

DO NOT use Coin Cells for WLAN_VBAT rail. They are designed for low power device (<10mA), whereas the CYW43438 can consume up to 300mA average current

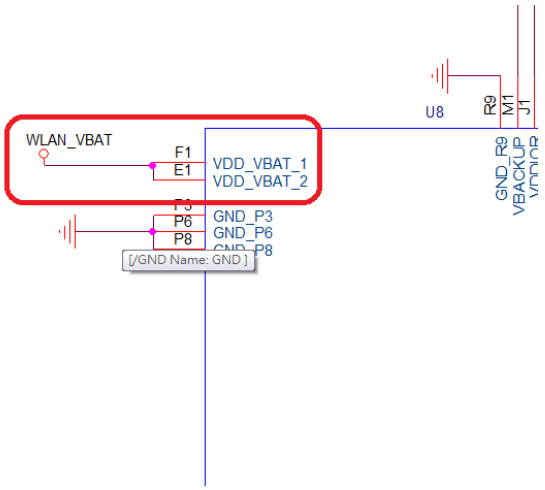


Figure 2

2.2 CapSense

Recommend use Port 8 (see Table 2) for its low self-capacitance inside the module

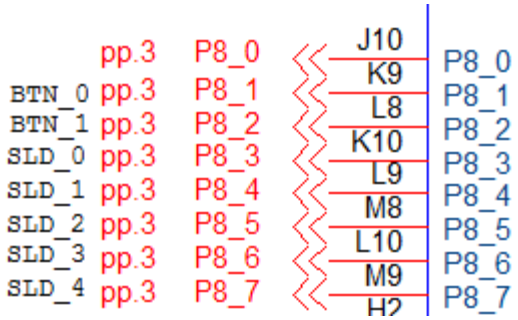


Figure 3

Every CapSense controller pin has some parasitic capacitance associated with it, adding an external resistor closed to the module (560 Ω for Self-capacitance and 2 kΩ for Mutual-capacitance) forms a low-pass RC filter that attenuates the RF noise amplitude coupled to the pin.

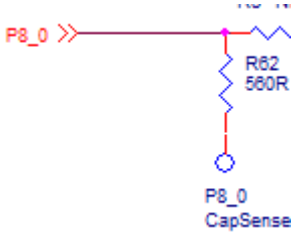


Figure 4

The simulation example below shows the mutual capacitance with different finger/sensor distance. Please evaluate your application and the capacitance requirement of the sensor provided by Infineon (refer to AN85951 - PSoC® 4 and PSoC® 6 MCU CapSense® Design Guide) along with our module pin parasitic capacitance shown in 2.4 P Pin parasitic capacitance to decide which sensing method suits your needs.

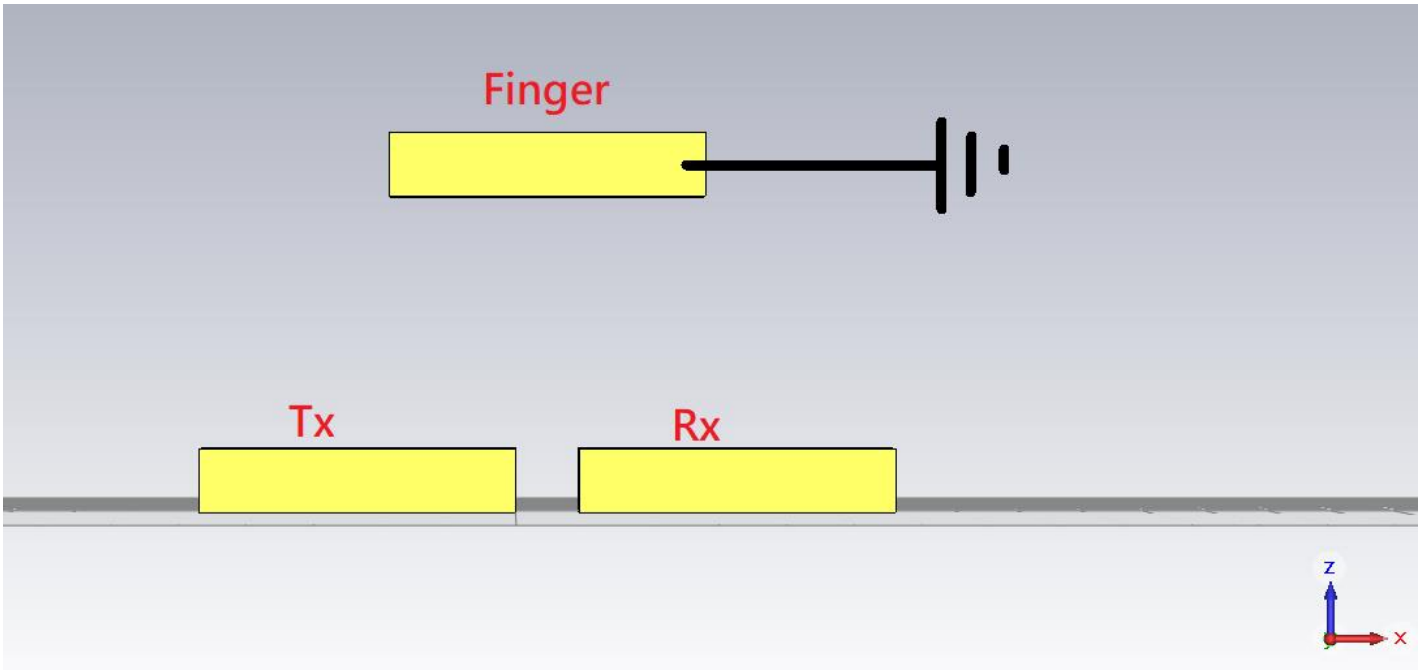


Figure 5

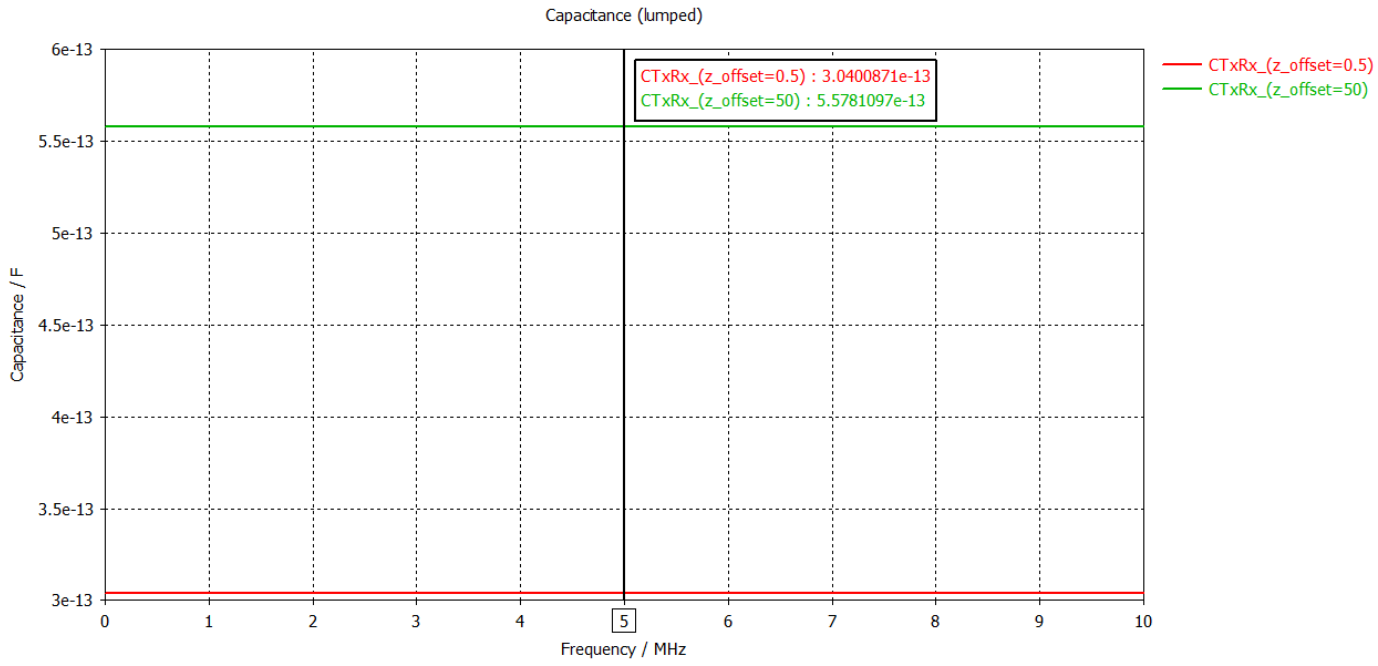


Figure 6

2.3 Debug Pins

Please leave the debug pins floating

Pin No	Definition	Basic Description
D5	BT_REG_ON	Reserved for debug use only
B1	BT_UART_CTS	Reserved for debug use only
D2	BT_UART_RTS	Reserved for debug use only
C2	BT_UART_RXD	Reserved for debug use only
B2	BT_UART_TXD	Reserved for debug use only
H4	SDIO_CLK_TP	Floating Pin, No connect to anything.
G5	SDIO_CMD_TP	Floating Pin, No connect to anything.
H5	SDIO_DATA0_TP	Floating Pin, No connect to anything.
G4	SDIO_DATA1_TP	Floating Pin, No connect to anything.
H7	SDIO_DATA2_TP	Floating Pin, No connect to anything.
H6	SDIO_DATA3_TP	Floating Pin, No connect to anything.
D6	WL_GPIO1	Reserved for debug use only
E6	WL_GPIO2	Reserved for debug use only
C1	WL_REG_ON	Reserved for debug use only

Table 1

2.4 P Pin parasitic capacitance

Pin No.	Definition	Parasitic capacitance (pF)
K6	P0_2	1
J7	P0_3	1.1
K7	P0_4	0.9
J6	P0_5	0.8
M2	P1_0	1.2
M3	P1_1	0.9
K3	P1_2	1.1
L3	P1_3	0.8
L2	P1_4	0.9
J3	P1_5	1
R7	P10_0	1.1
R6	P10_1	1
P7	P10_2	0.9
L6	P10_3	0.9

N7	**P10_4**	0.8
M7	**P10_5**	0.7
M6	**P10_6**	0.7
R4	**P11_0**	1.4
L4	**P11_1**	1.2
R5	**P11_2**	1
N6	**P11_3**	0.7
M4	**P11_4**	1.1
P4	**P11_5**	1.1
P5	**P11_6**	0.9
M5	**P11_7**	0.8
R2	**P12_0**	1.5
R1	**P12_1**	1.8
N1	**P12_2**	1.7
P1	**P12_3**	1.6
P2	**P12_4**	1.5
N2	**P12_5**	1.3
C4	**P5_0**	2.2
F4	**P5_1**	1.3
E4	**P5_2**	1.4
F5	**P5_3**	1.1
D4	**P5_4**	1.9
B5	**P5_5**	2.4
B4	**P5_6**	2.3
C5	**P5_7**	2.2
F7	**P6_0**	1
E7	**P6_1**	1.2
E8	**P6_2**	1.3
G8	**P6_3**	0.9
F8	**P6_4**	0.9
E9	**P6_5**	1.2
E10	**P6_6**	1.3
D10	**P6_7**	1.5
F10	**P7_0**	1.2
H9	**P7_3**	0.6

G9	**P7_4**	1
G10	**P7_5**	1.3
J10	**P8_0**	0.7
K9	**P8_1**	0.5
L8	**P8_2**	0.4
K10	**P8_3**	0.7
L9	**P8_4**	0.4
M8	**P8_5**	0.6
L10	**P8_6**	0.6
M9	**P8_7**	0.5
P9	**P9_0**	0.9
N9	**P9_1**	0.7
M10	**P9_2**	0.6
N8	**P9_3**	0.8
P10	**P9_4**	0.9
N10	**P9_5**	0.7
R10	**P9_6**	1.1

Table 2